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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/501,391 | 07/15/2004 | Michitaro Kanamitsu | XA-10097 | 2499 |

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MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

| EXAMINER | |
|---|---|
| TRAN, MICHAEL THANH | |
| **ART UNIT** | **PAPER NUMBER** |
| 2827 | |

DATE MAILED: 03/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/501,391 | KANAMITSU ET AL. | |
| | Examiner | Art Unit | |
| | Michael t. Tran | 2827 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *July 15, 2004 through January 19, 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5 and 6* is/are rejected.

7)☒ Claim(s) *2-4 and 7-12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *071504*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

MICHAEL TRAN
PRIMARY EXAMINER

# DETAILED ACTION

1. In response to the Communications dated July 15, 2004 through January 19, 2005, claims 1-12 are active in this application.

## *Foreign Priority*

2. No claim of Foreign Priority being made.

## *Information Disclosure Statement*

3. The information disclosure statement filed July 15, 2004 has been considered.

## *Claim Objections*

4. Claims 2-4 and 7-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The claim language and the drawing disclosure appear to contradict each other. In claim 1, it appears that the claim calls for only one sense latch circuit for one particular memory cell with corresponding word line and bit line. However, figure 3 of the disclosure shows that there is only one sense latch circuit coupled to a global bit line, which is being applied to an entire array of memory cells. Recitations of claim 5 appears to match with the drawing disclosure.

***Claim Rejections – 35 U.S.C. § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

6. Claims 1, 5, and 6 are rejected, as understood, under 35 U.S.C 102(b) as being anticipated by Sato et al. [U.S. Patent #6,026,014].

With respect to claim 1, Sato et al. disclose, in figure 4, a nonvolatile semiconductor storage unit comprising: a plurality of word lines [WLmn]; a plurality of bit lines [this is being interpreted as being the global bit line [Blu – see the above remarks]; a plurality of memory cells [MCC] each of which is correspondingly connected to one word line and one bit line and has a control gate and a floating gate [see the above remarks regarding the bit line recitations]; a sense latch circuit [SL] which is connected to one end of said bit line and detects data on said bit line correspondingly to a threshold voltage of said memory cell; a MOSFET [Q.sub.p1] which is connected between said bit line and said sense latch circuit, uses its gate to receive data on said bit line, and drives a node for said sense latch circuit; a bit line precharge circuit

[Q.sub.p2] which is connected to said bit line and precharges said bit line; and a power supply circuit [Q.sub.c1] which is connected to said bit line precharge circuit and generates precharge voltage for said bit line dependently on a threshold voltage of said MOSFET. See column 9.

With respect to claim 5, Sato et al. disclose the plurality of memory cells are commonly connected to a common line via a MOSFET [Q.sub.s1 of figure 4] whose source is driven by a gate control signal [SDL_U of figure 4], and wherein a gate of each memory cell is connected to each word line [see figure 4] and a drain thereof is commonly connected to a bit line [see figure 4].

With respect to claim 6, Sato et al. disclose that each of said plurality of memory cells can store a plurality of bits of data as a threshold voltage [see abstract].

### *Allowable Subject Matter*

7. The following is an Examiner's statement of reasons for the indication of allowable subject matter: the prior art of records does not show (in addition to the other elements in the claim) the following:

- Wherein said bit line precharge circuit can supply first and second potentials with different voltage values and further comprises a function to discharge said bit line, wherein said bit line precharge circuit is supplied with said first potential when precharging said bit line, and wherein said bit line precharge circuit is supplied with said second potential when discharging said bit line.

- Wherein said selection circuit can supply fifth and sixth potentials with different voltage values and further comprises a function to precharge and discharge the node for said sense latch circuit, wherein said selection circuit makes connection between said sense latch circuit and said common input/output line when data is exchanged therebetween, wherein said selection circuit is supplied with said fifth potential when the node for said sense latch circuit is precharged, and wherein said selection circuit is supplied with said sixth potential when the node for said sense latch circuit is discharged.

***Conclusion***

8. When responding to the Office action, Applicants are advised to provide the Examiner with line and page numbers of the application and/or references cited to assist the Examiner in the prosecution of this case.

9. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Michael T. Tran whose telephone number is (571) 272-1795. The Examiner can normally be reached on Monday-Thursday from 7:30-6:00 P.M.

10. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-1650.

Michael T. Tran
Art Unit 2827
March 22, 2005

MICHAEL TRAN
PRIMARY EXAMINER